Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-18 (Cancelled)

19. (Currently Amended) An integrated circuit including at ~~lest~~ least one transistor, the integrated circuit comprising:

a pair of local interconnects spaced from each other by a minimum lithographic feature and each being a minimum lithographic feature; and

a gate of the transistor disposed in the space between the local interconnects and separated from each of the local interconnects by an insulating liner, wherein the space is less than or equal to the minimum lithographic feature, whereby the width of the transistor is not greater than three of the minimum lithographic features.

20. (Currently Amended) The integrated circuit of Claim 19, wherein the insulating ~~spacers are each~~ liner is disposed on ~~a~~ an interconnect wall adjacent the gate to separate each of the local interconnects from the gate.

21. (Previously Presented) An integrated circuit including at least one transistor, the integrated circuit comprising:

a pair of local interconnects spaced from each other; and

a gate of the transistor disposed in the space between the local interconnects and separated from each of the local interconnects by an insulating liner, wherein the space is less than or equal to one minimum lithographic feature.

22. (Original) The integrated circuit of Claim 21, wherein the pair of local interconnects are spaced from each other by a minimum lithographic feature.

23. (Previously Presented) The integrated circuit of claim 21, wherein the insulating liners are each disposed on an interconnect wall adjacent the gate to separate each of the local interconnects from the gate.

24. (Previously Presented) The integrated circuit of claim 21, wherein a source and drain are disposed by at least partially beneath the insulating liners.

25. (Previously Presented) An integrated circuit including at least a pair of local interconnects with one interconnect on each side of a gate of a transistor, the integrated circuit being manufactured by a method comprising steps of:

forming on a semiconductor substrate a thick insulating layer;

forming at least a pair of spaced apart openings in the insulating layer adjacent the semiconductor substrate;

forming a source in one of the openings and a drain in the other of the openings;

filling each of the openings with a conductive material to form the local interconnects, the local interconnects being electrically coupled to the source and drain;

removing a portion of the insulating layer to form a gate opening between the local interconnects;

forming a gate dielectric on the semiconductor substrate in the gate opening; and

forming the gate on the gate dielectric in the gate opening between the local interconnects.

26. (Previously Presented) The integrated circuit of Claim 25, wherein the space between the pair of openings is one minimum photolithographic feature and the local interconnects are each one minimum photolithographic feature.

27. (Previously Presented) The integrated circuit of Claim 25, wherein insulating spacers are each disposed on an interconnect wall adjacent the gate to separate each of the local interconnects from the gate.

28. (Previously Presented) The integrated circuit of Claim 25, wherein the source and drain are formed by implanting impurities in the pair of openings in the insulating layer.

29. (Previously Presented) The integrated circuit of Claim 25, wherein the portion of insulating layer removed to form the gate opening is removed by using a masking material with an opening in the masking material positioned between the pair of local interconnects.

30. (Previously Presented) The integrated circuit of Claim 29, wherein the opening in the masking material extends over but not beyond each of the pair of local interconnects.

31. (Previously Presented) The integrated circuit of Claim 30, wherein the opening in the masking material is positioned over an active region in the semiconductor substrate, the active region being surrounded by an isolation region, the opening in the masking material extending to or beyond the active region.

32. (Previously Presented) The integrated circuit of Claim 25, wherein a conductive layer is formed on walls of the to line the spaced apart openings and a remainder of the spaced apart openings are filled with another conductive material.

33. (Previously Presented) The integrated circuit of Claim 25, wherein the conductive material includes polysilicon and tungsten.

34. (Previously Presented) The integrated circuit of Claim 33, wherein the polysilicon is the origin for the impurities for the source and drain.

35. (Previously Presented) The integrated circuit of Claim 25, wherein a barrier layer is formed on the walls of the spaced apart openings to line the opening and a remainder of the local interconnect opening is filled with a conductive material.

36. (Previously Presented) The integrated circuit of Claim 35, wherein the barrier layer includes titanium nitride.

37. (Previously Presented) The integrated circuit of Claim 25, wherein an insulating etch stop layer is formed on semiconductor substrate before forming the thick insulating layer.

38. (Previously Presented) The integrated circuit of Claim 37, wherein the etch selectivity of the etch stop layer is different from the etch selectivity of the insulating layer.